REMARKS

In the Advisory Action (mailed August 8, 2004), the Examiner sustained the claim

rejections of the previous Final Office Action (mailed February 13, 2004). In the previous Final

Office Action, the Examiner rejected claims 1-18 under § 102 as being anticipated by USP

5,742,086 issued to Rostoker et al. (Rostoker). In this Preliminary Amendment, Applicants have

amended claims 1, 3, 4, 6, 10, 12, 14, and 15. No claims have been added or canceled.

Accordingly, claims 1-18 will be pending after entry of this Preliminary Amendment.

Reconsideration of the present application in view of the following remarks is respectfully

requested.

I. Claims 1-9

The Examiner rejected claims 1-9 under § 102 as being anticipated by Rostoker.

Claims 2-9 are dependent directly or indirectly on independent claim 1. Claim 1 recites a

method of placing a set of circuit elements in the circuit layout for a placer that partitions a

region of a circuit layout into several sub-regions. This method identifies during a placement

operation, for a set of sub-regions that contain the circuit elements, a connection graph that

connects the set of sub-regions. The connection graph has at least one edge that is at least

partially diagonal. The method identifies a placement cost from an attribute of the connection

graph. The placement cost specifies a cost for the placement of the circuit elements. The method

uses the placement cost, during a placement operation, to identify a placement for the circuit

elements. The placement specifies positions in the circuit layout for the circuit elements.

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Cadence Reference Number: 2002-077 P 05 PTO Serial Number: 10/079,270 Applicants respectfully submit that Rostoker does not disclose teach, or even suggest

such a method. The Examiner identifies Figure 71 and column 59 of Rostoker as disclosing the

identification of a connection graph during a placement operation limitation of claim 1. These

passages of Rostoker, however, disclose a "three directional/diagonal routing Steiner tree"

implemented during a routing operation. This Steiner tree as disclosed in Rostoker is not

identified during a placement operation. Therefore, Rostoker does not disclose, teach or even

suggest the recited method of claim 1 that identifies, during a placement operation, a connection

graph that connects the set of sub-regions.

The Examiner identifies column 58, column 43 lines 22-30, column 44 lines 46+, and

column 45 lines 21-26 of Rostoker as disclosing the identification of a placement cost from an

attribute of the connection graph limitation of claim 1. These passages of Rostoker, however,

disclose computing costs without reference to an attribute of a connection graph. These costs are

computed prior to the identification of the "three-directional/diagonal routing Steiner tree,"

which the Examiner cites as a connection graph. Therefore, Rostoker does not disclose, teach, or

even suggest the recited method of claim 1 which, after identifying a connection graph, identifies

a placement cost from an attribute of the connection graph.

Moreover, Applicants have amended claim 1 to recite a method that uses the placement

cost during a placement operation to identify a placement for the circuit elements, where the

placement specifies positions in the circuit layout for the circuit elements. Rostoker does not

disclose, teach, or even suggest this limitation of claim 1 because, as mentioned above, Rostoker

does not identify a connection graph during a placement operation, or identify a placement cost

from an attribute of the connection graph during a placement operation.

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Cadence Reference Number: 2002-077 P 05 PTO Serial Number: 10/079,270 Accordingly, Applicants respectfully submit that Rostoker does not render claim 1

unpatentable. As claims 2-9 are dependent on claim 1, Applicants respectfully submit that claims

2-9 are patentable over Rostoker for at least the same reasons. In view of the foregoing,

Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims

1-9.

II. Claims 10-18

The Examiner rejected claims 10-18 under § 102 as being anticipated by Rostoker.

Claims 11-18 are dependent directly or indirectly on independent claim 10. Claim 10

recites a computer readable medium that stores a program for placing a set of circuit elements in

the circuit layout. This computer program is for a placer that partitions a region of a circuit layout

into several sub-regions. The computer program has a first set of instructions for identifying

during a placement operation, for a set of sub-regions that contain the circuit elements, a

connection graph that connects the set of sub-regions. The connection graph has at least one edge

that is at least partially diagonal. The computer program has a second set of instructions for

identifying a placement cost from an attribute of the connection graph. The placement cost

specifies a cost for the placement of the circuit elements. The computer program has a third set of

instructions for using the placement cost, during a placement operation, to define a position in

the in the circuit layout for the circuit elements.

Applicants respectfully submit that Rostoker does not disclose teach, or even suggest

such a computer program. The Examiner identifies Figure 71 and column 59 of Rostoker as

disclosing the identification of a connection graph during a placement operation limitation of

claim 10. These passages of Rostoker, however, disclose a "three directional/diagonal routing

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Steiner tree" implemented during a routing operation. This Steiner tree as disclosed in Rostoker

is not identified during a placement operation. Therefore, Rostoker does not disclose, teach or

even suggest the recited computer program of claim 10 that identifies, during a placement

operation, a connection graph that connects the set of sub-regions.

The Examiner identifies column 58, column 43 lines 22-30, column 44 lines 46+, and

column 45 lines 21-26 of Rostoker as disclosing the identification of a placement cost from an

attribute of the connection graph limitation of claim 10. These passages of Rostoker, however,

disclose computing costs without reference to an attribute of a connection graph. These costs are

computed prior to the identification of the "three-directional/diagonal routing Steiner tree,"

which the Examiner cites as a connection graph. Therefore, Rostoker does not disclose, teach, or

even suggest the recited computer program of claim 10 which, after identifying a connection

graph, identifies a placement cost from an attribute of the connection graph.

Moreover, Applicants have amended claim 1 to recite a method that uses the placement

cost during a placement operation to define a position in the circuit layout for the circuit

elements. Rostoker does not disclose, teach, or even suggest this limitation of claim 10 because,

as mentioned above, does not identify a connection graph during a placement operation, or

identify a placement cost from an attribute of the connection graph during a placement operation.

Accordingly, Applicants respectfully submit that Rostoker does not render claim 10

unpatentable. As claims 11-18 are dependent on claim 10, Applicants respectfully submit that

claims 11-18 are patentable over Rostoker for at least the same reasons. In view of the foregoing,

Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims

10-18.

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CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1-18, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted

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